

Vu Hoang (Gary) Pham

Philadelphia, PA, 19104 • 267-455-3394

hoangvuph03@gmail.com • [Github.com/kagamirudo](https://github.com/kagamirudo) • [Linkedin.com/in/gary-pham/](https://www.linkedin.com/in/gary-pham/)

Education

Drexel University, Pennoni Honors College, College of Engineering

Philadelphia, PA

M.S in Computer Engineering

Graduation: Jun 2027

B.S in Computer Science, Minors in Computer Engineering & Mathematics

Graduated: Jun 2025

Concentrations: Computer System & Architecture, Algorithms & Data Structure

GPA: 3.85 - Dean's List

Skills

Languages: C, C++, Python, Java, Racket, Haskell, Bash, Kotlin, Go, Rust, Pascal, SQL, Assembly (x86)

Tools: CUDA, CMake, VsCode, IntelliJ, Git, UNIX, CCS, Arduino, UML, DrRacket, Docker, AWS, Clang, GCC

Systems: Windows, Linux (Ubuntu, Mint, Kali, Raspberry Pi), MacOS, Plan 9, Android

Frameworks: Django, Node.js, Angular, Spring

Work Experience

ImesPro, Edge AI & Factory Automation

Ho Chi Minh, Vietnam

Internship Embedded Software Engineer

Jun 2026 - Present

- Developed ESP32-S3-CAM factory automation firmware in C/ESP-IDF with **ThingsBoard MQTT** (telemetry, RPC, OTA), multi-task FreeRTOS (camera, OCR uploader, health), and **double-buffered frame** upload to an OCR backend for on-line visual inspection.
- Engineered edge CV on **ESP32-S3-CAM (ESP-DL)** and **Luckfox Pico Pro (RKNN)**: trained PyTorch digit CNN, quantized **INT8** via **esp-ppq**, deployed on-device OCR with digit segmentation at **~10 FPS**; ran **YOLO11n** on **RV1106 NPU** with RGA letterbox at **~8-12 FPS**; shipped production QR and face firmware with dual-core **FreeRTOS**, **≥15 FPS** capture, and **MQTT** event publishing.
- Researched SmartClass inattention pipeline (YOLOv8, ByteTrack, MediaPipe) at **15-30 FPS on CPU**, exported YOLO to ONNX for Jetson TensorRT deploy, and evaluated YOLO fine-tuning on classroom datasets for tiered ESP32-gateway analytics.

Drexel University

[Drexel Material Lab](#)

Embedded Software Engineer

Nov 2025 - May 2026

- Developed an **ESP32-S3 embedded data acquisition system** in C/ESP-IDF for laser-material experiments, sampling **12-bit ADC signals at 3 kHz**, generating **5 kHz PWM** laser control, and supporting **10M-sample** capture sessions.
- Engineered a **dual-core FreeRTOS pipeline** with a **48k-entry SPIRAM queue (~16 s buffer at 3 kHz)** and **500-sample batched CSV writes**, improving logging reliability during SD-card and network I/O
- Built a **browser-based control and data delivery stack** with live telemetry, start/stop APIs, **50 s chunked downloads**, SD/SPIFFS failover, synchronized timestamps, and **30 s benchmark-mode CSV/binary** throughput testing.

Medcrypt

Solana Beach, CA, US

CO-OP Embedded Software Engineer

Apr 2024 - Sep 2024

- Designed and implemented an optimized ASN.1 encoder/decoder in C for STM32 microcontrollers, reducing the firmware footprint by **30%** (from 64 KB to 45 KB) and boosting encoding throughput by **40%**.
- Identified and resolved **150,000+ namespace symbol** conflicts in a **2 MB vendor codebase**, eliminating CI build failures and cutting integration **debugging time by 50%**.
- Unified hardware-accelerated AES encryption on the STM32 platform, slashing cryptographic **processing latency by 25%** and ensuring deterministic performance for real-time data protection.

FPT Software, OCR Quy Nhon Team

Hanoi, Vietnam

Internship A.I Researcher & Engineer

Jun 2022 - Sep 2022

- Fine-tuned a CNN OCR pipeline on 50k Japanese Kanji samples, raising accuracy **77% to 92%**.
- Pruned and quantized the model, cutting inference **200 ms down to 80 ms (-60%)** for real-time edge OCR.
- Integrated OCR into an Angular web app, processing up to **2000 scanned images per minute** and tripling throughput in end-user.

Research

FPGA Compiler for Nested Loop Acceleration

[Drexel Master Research](#)

Hardware Researcher

Jun 25 - Present

- Designed LU decomposition and matrix factorization arrays on Xilinx FPGA (Zybo Z) using Vitis HLS and AXI-Stream IP, **achieving x2.3 speedup** over baseline C implementation.
- Compiled nested loop kernels into 64-PE arrays with **> 90% pipeline utilization** and verified through cycle-accurate simulation.
- Evaluated synthesis results via C/C++ and VHDL testbenches, optimizing DMA throughput by **35%** through bus-width and latency tuning.

Lexicographically Minimum String Rotation

[Drexel Senior Project](#)

Quantum Researcher

Sep 24 - Jun 25

- Architected and implemented a quantum LMSR algorithm in **Qiskit** using **Grover's amplification**, reducing theoretical search complexity from $O(N \log N)$ to $O(\sqrt{N})$ for N qubits this translates to **~320 fewer oracle calls**.
- Simulated and deployed the **6-qubit LMSR circuit** on IBM Quantum hardware, executing **100 runs across 20 problem instances** with an average **≥ 97% success rate**, and validated against classical benchmarks.
- Applied the algorithm to benzenoid edge code recognition over **50 molecular graphs** for Drexel's Week of Excellence, slashing end-to-end **processing time by 30%**.

Activities

Participant, ICPC USA Regional Contest, Philly Code Fest, DragonHack

Varsity Player, Drexel Badminton Club, Hanoi Swimming Team